CLAIMS

What is claimed is:

1. A chip comprising:

transmitters to provide transmit signals to chip interfaces;

voltage control circuitry to control voltages of the transmit signals;

receivers to receive external signals from another chip; and

evaluation circuitry to determine whether the transmit signals were usable by the other chip based on an evaluation of at least one of the received external signals and to provide a usability indicating signal to the voltage control circuitry indicative of whether the transmit signals were usable by the other chip.

2. The chip of claim 1, wherein if the usability indicating signal indicates the transmit signals were usable by the other chip, the voltage control circuitry lowers voltages of subsequent transmit signals.

3. The chip of claim 1, wherein if the usability indicating signal indicates the transmit signals were not usable by the other chip, the voltage control circuitry raises voltages of subsequent transmit signals to voltages of previous transmit signals that were determined to be usable by the other chip.

4. The chip of claim 1, wherein the evaluation circuitry and the voltage control circuitry operate to find a lowest available usable voltage for the voltages of the transmit signals.

5. The chip of claim 1, wherein the external signals include looped back signals of at least portions of the transmit signals and are provided by the other chip to the receivers, and wherein the evaluation circuitry compares at least portions of the looped back signals to at least partial representations of the transmit signals.

6. The chip of claim 1, wherein if the at least one of the received external signals includes a retry request, the evaluation circuitry determines whether a number of received retry requests is within an acceptable level.

7. The chip of claim 6, wherein if the number of received retry signals is not within the acceptable level, the usability indicating signal indicates that the transmit signals were not usable by the other chip.

8. The chip of claim 6, wherein the received the number of retry signals must be within an acceptable level for a variety of test patterns for the evaluation circuitry to conclude that the transmit signals were usable.

9. The chip of claim 1, wherein the evaluation is done during an initialization mode and then not repeated until another initialization.

10. The chip of claim 1, wherein the evaluation is done during an initialization mode and the initialization mode can be entered by one or more of the following: the chip being first given power, a chip being reset, in response to a particular number of retry requests being received, a temperature exceeding a threshold, and a change in a power source.

11. The chip of claim 1, wherein the transmit signals are part of a test routine and the other chip determines whether the test routine is correct and provides a pass or fail signal as part of the external signals, and wherein the evaluation circuitry uses the pass or fail signal in determining whether the transmit signals were usable by the other chip.

12. The chip of claim 1, wherein the voltage control circuitry changes the voltages of the transmit signals prior to there being received by the transmitter.

13. The chip of claim 1, wherein the transmitter changes the voltages of the transmit signals under the control of the voltage control circuitry.

14. The chip of claim 1, wherein if any of the transmit signals are determined to have been unusable, then the voltages are changed for all of the transmit signals.

15. A chip comprising:

a transmitter to provide a transmit signal to at least one chip interface;

voltage control circuitry to control a voltage of the transmit signal;

a receiver to receive an external signal from another chip; and

evaluation circuitry to determine whether the transmit signal was usable by the other chip based on an evaluation of the received external signal and to provide a usability indicating signal to the voltage control circuitry indicative of whether the transmit signal was usable by the other chip.

16. The chip of claim 15, wherein if the usability indicating signal indicates the transmit signal was usable by the other chip, the voltage control circuitry lowers the voltage of a subsequent transmit signal.

17. The chip of claim 15, wherein if the usability indicating signal indicates the transmit signal was not usable by the other chip, the voltage control circuitry raises voltages of a subsequent transmit signal to a voltage of a previous transmit signals that was determined to have been usable by the other chip.

18. The chip of claim 15, wherein the evaluation circuitry and the voltage control circuitry operate to find a lowest available usable voltage for the voltages of the transmit signals.

19. The chip of claim 15, wherein the external signal may include one of the following: a looped back signal, a retry request, or a pass or fail signal.

20. A chip comprising:

transmitters to provide transmit signals to chip interfaces;

control circuitry to control power of the transmit signals;

receivers to receive external signals from another chip; and

evaluation circuitry to determine whether the transmit signals were usable by the other chip based on an evaluation of at least one of the received external signals and to provide a usability indicating signal to the control circuitry indicative of whether the transmit signals were usable by the other chip.

21. The chip of claim 20, wherein if the usability indicating signal indicates the transmit signals were usable by the other chip, the control circuitry lowers power of subsequent transmit signals.

22. The chip of claim 20, wherein if the usability indicating signal indicates the transmit signals were not usable by the other chip, the control circuitry raises power of subsequent transmit signals to power of previous transmit signals that were determined to be usable by the other chip.

23. The chip of claim 20, wherein the evaluation circuitry and the voltage control circuitry operate to find a lowest available usable power for the power of the transmit signals.

24. A system comprising:

first and second interconnects;

first and second chips coupled by the first and second interconnects;

wherein the first chip includes:

transmitters to provide transmit signals to first interconnects;

voltage control circuitry to control voltages of the transmit signals;

receivers to receive external signals from the second chip; and

evaluation circuitry to determine whether the transmit signals were usable by the second chip based on an evaluation of at least one of the received external signals and to provide a usability indicating signal to the voltage control circuitry indicative of whether the transmit signals were usable by the second chip.

25. The system of claim 24, wherein if the usability indicating signal indicates the transmit signals were usable by the second chip, the voltage control circuitry lowers voltages of subsequent transmit signals.

26. The system of claim 24, wherein if the usability indicating signal indicates the transmit signals were not usable by the second chip, the voltage control circuitry raises voltages of subsequent transmit signals to voltages of previous transmit signals that were determined to be usable by the second chip.

27. The system of claim 24, wherein the evaluation circuitry and the voltage control circuitry operate to find a lowest available usable voltage for the voltages of the transmit signals.

28. The system of claim 24, wherein the external signals include looped back signals of at least portions of the transmit signals and are provided by the second chip to the receivers, and wherein the evaluation circuitry compares at least portions of the looped back signals to at least partial representations of the transmit signals.

29. The system of claim 24, wherein if the at least one of the received external signals includes a retry request, the evaluation circuitry determines whether a number of received retry requests is within an acceptable level.

30. The system of claim 24, wherein the evaluation is done during an initialization mode and then not repeated until another initialization.

31. The system of claim 24, wherein the evaluation is done during an initialization mode and the initialization mode can be entered by one or more of the following: the first chip being first given power, a first chip being reset, in response to a particular number of retry requests being received, a temperature exceeding a threshold, and a change in a power source.

32. The system of claim 24, wherein the transmit signals are part of a test routine and the second chip determines whether the test routine is correct and provides a pass or fail signal as part of the external signals, and wherein the evaluation circuitry uses the pass or fail signal in determining whether the transmit signals were usable by the second chip.